METHOD FOR IMPROVING RELIABILITY OF COPPER INTERCONNECTS

FIELD OF THE INVENTION

[0001] The invention is generally related to the field of forming damascene copper interconnects in semiconductor devices and more specifically to improving the reliability of damascene copper interconnects.

BACKGROUND OF THE INVENTION

[0002] As the density of semiconductor devices increases, the demands on interconnect layers for connecting the semiconductor devices to each other also increases. Therefore, device fabrication technology is migrating from aluminum metal interconnects to copper interconnects and from traditional silicon-dioxide-based dielectrics to low-k dielectrics, such as organo-silicate glass (OSG). Semiconductor fabrication processes that work with copper interconnects and newer low-k dielectrics are still being developed and optimized. As compared to the traditional subtractive plasma dry etching of aluminum, suitable copper etches for a semiconductor fabrication environment are not readily available. To overcome the copper etch problem, damascene processes have been developed.

[0003] In a damascene process, the IMD (intrametal dielectric) is formed first. The IMD is then patterned and etched to form a trench for the interconnect line. If connection vias have not already been formed, a dual damascene process may be used. In a dual damascene process, vias are etched into the ILD (interlevel dielectric) 12 for connection to lower interconnect levels and trenches are etched into the IMD 14. The barrier layer 16 and a copper seed layer are then deposited over open via/trench structures. The barrier layer 16 is typically tantalum nitride or some other binary

transition metal nitride and the thin Cu seed layer is deposited using physical vapor deposition. A copper layer is then electrochemically deposited onto the seed layer that covers the entire structure. The copper is then chemically-mechanically polished (CMP'd) to remove the copper over the IMD 14, leaving copper interconnect lines 18 and vias 20 as shown in FIG. 1. A metal etch is thereby avoided.

[0004] Typically, several copper interconnect layers are successively formed. After one metal interconnect layer is formed, an etchstop layer is deposited thereover and the next levels' ILD and IMD are formed. The etchstop layer prevents Cu diffusion from the metal lines into the overlying oxide-based dielectric and protects the Cu from subsequent via/trench etches used to form the next level of interconnect.

SUMMARY OF THE INVENTION

[0005] The invention is a method for forming a copper interconnect having improved reliability. After the copper is plated by electrochemical deposition (ECD) and chemically-mechanically polished back, the exposed copper surface is lightly doped with silicon by flowing a silicon containing gas such as SiH_4 over the wafer surface immediately prior to depositing the overlying dielectric layer. Silicon doping improves electromigration (EM) and via stress migration (VSM) lifetimes by slowing the Cu diffusion rate at the interface between the Cu leads and the overlying dielectric barrier.

[0006] An advantage of the invention is providing a copper interconnect having improved reliability using a method that requires no additional equipment beyond what is normally required to create such interconnects.

[0007] This and other advantages will be apparent to those of ordinary skill in the art having reference to the specification in conjunction with the drawings.

[0008] BRIEF DESCRIPTION OF THE DRAWINGS

[0009] In the drawings:

[0010] FIG. 1 is a cross-sectional diagram of a conventional (prior art) dual damascene copper interconnect.

[0011] FIG. 2 is a cross-sectional diagram of a copper interconnect formed according to an embodiment of the invention.

[0012] FIGs. 3A-3E are cross-sectional diagrams of the copper interconnect of FIG. 2 at various stages of fabrication.

[0013] FIG. 4 shows EM lifetime improvement under stress conditions of 325°C and 1.5MA/cm^2 current density for cases of 1) no silane over wafer prior to SiN deposition and 2) 3 seconds silane over wafer prior to SiN deposition.

[0014] FIG. 5 is a graph of Via Stress Migration improvement with SiH4 exposure and temperature. Increased SiH4 flow or increased temperature result in increased Si doping level of the Cu surface.

[0015] FIG. 6 is a graph depicting the interface adhesion energy (as determined by 4-point bending methodology) for the case of various doping conditions. The interface strength improves with higher doping levels.

[0014] DETAILED DESCRIPTION OF THE EMBODIMENTS

[0015] The invention will now be described in conjunction with a specific via first copper dual damascene process. It will be apparent to those of ordinary skill in the art that the benefits of the invention may be applied to other copper interconnect processes such as single damascene processes, trench first dual damascene processes and other via first dual damascene processes.

[0016] As the technology scales to below the 130 nm node, the VSM and EM requirements become more and more difficult to meet. The inventors have discovered that by doping the copper interconnect with a small amount of Si after CMP improves the VSM and EM lifetimes. FIG 4 shows the EM lifetime improvement for a Si-doped vs. undoped interconnect line of ~0.18 μm width and ~0.35 μm depth under stress conditions of 325°C and 1.5MA/cm^2. FIG 5 shows the improvement in Via Stress Migration 48hr/150C shift for the case of 0 seconds or 3 seconds SiH_4 flow at 400C and 3 seconds SiH_4 flow at 425C. The EM and VSM improvements are attributed to the improvement in adhesion interface energy between the SiN and the Si-doped Cu, shown in FIG 6.

[0017] A dual damascene copper interconnect 100 formed according to the invention is shown in FIG. 2. Copper interconnect 100 is formed over semiconductor body 102. Semiconductor body 102 typically has transistors and other devices (not shown) formed therein. Semiconductor body 102 may also include one or more additional metal interconnect layers (not shown). Copper interconnect 100 comprises a lead portion formed within trenches 108. A via portion is formed in vias 106 below trenches 108. Vias 106 extend from the bottom of trenches 108 through interlevel dielectric (ILD) 110 to a lower metal interconnect layer. Trenches 108 are formed within intrametal dielectric (IMD) 112. Various materials are known to be suitable for forming ILD 110 and IMD 112. For example,

fluorine-doped silicate glass (FSG), organo-silicate glass (OSG), or other low-k or ultra low-k dielectrics may be used.

[0018] A metallic barrier layer 114 is located between the copper interconnect 100 and the trench 108 and via 106 sidewalls. Barrier layer 114 prevents copper from diffusing into the ILD 110 and IMD 112. Barrier layer 114 also provides adhesion between the copper and dielectric. Various barrier layers are known in the art. For example, refractory metals, refractory metal-nitrides, refractory metal-silicon-nitrides, or combinations thereof may be used.

[0019] Copper interconnect 100 of the preferred embodiment includes Si dopant 115. As discussed further below, doping with Si occurs after copper CMP. Accordingly, Si dopant 115 is gaseously introduced over the surface of copper interconnect 100. The concentration of the as deposited Si dopant is approximately 0.1% Si. As discussed above, doping the copper interconnect 100 with Si improves the EM and VSM lifetimes.

[0020] A method of fabricating copper interconnect 100 according to the invention will now be discussed with reference to Figs. 3A-3E. Referring to Fig. 3A, semiconductor body 102 is processed through the formation of one or more metal interconnect layers. ILD 110 and IMD 112 are deposited over semiconductor body 102. Suitable materials, such as FSG or OSG, for ILD 110 and IMD 112 are known in the art. Trenches 108 are formed in IMD 112 and vias 106 are formed in ILD 110, using conventional processing.

[0021] Barrier layer 114 is formed over IMD 112 including within trenches 108 and vias 106. Barrier layer 114 functions as a diffusion barrier to prevent copper diffusion and as an adhesion layer. Transition metals and their nitrides are typically used for barriers. A transition metal-silicon nitride as well as combinations of transition metals, transition metal-nitrides and transition metal-silicon-nitrides may

also be used. As an example, barrier layer 114 may comprise a Ta-N based sputtered film.

[0022] Still referring to FIG. 3A, a copper seed layer 116 may be deposited over barrier layer 114. Physical vapor deposition is traditionally used to form copper seed layer 116. Other methods for forming copper seed layer 116, such as CVD are known in the art. Copper seed layer 116 is preferably undoped. The copper seed layer 116 is needed to pass current and to serve as a nucleation layer for the copper ECD process.

[0023] After deposition of the copper seed layer 116, the wafer is transferred to the ECD tool. Copper film 118 is formed by ECD. Various suitable ECD process are known in the art. In a preferred embodiment of the invention, the wafer is transferred to the plating cell of an ECD tool and a plating process is conducted. The plating step may include several plating currents as is well known in the art. The resulting copper film 118 is shown in FIG. 3B. While ECD copper is described herein, the invention is not limited to ECD deposited copper.

[0024] After the final copper thickness is achieved, the copper film 118 may be annealed. After the ECD process and any annealing steps, the copper layer 118 (which incorporates seed layer 116) and barrier layer 114 are chemically-mechanically polished to remove the excess material above a surface level of IMD 112. The remaining copper and barrier 114 in the trench forms copper interconnect 100, as shown in Fig. 3C.

[0025] After the copper CMP and prior to depositing any subsequent layers, such as the etchstop layer for the next metal interconnect level, the surface of copper interconnect 100 is doped with silicon, as shown in FIG. 3D. In the preferred embodiment of the invention, silicon doping is achieved in the same chamber used for depositing the subsequent etchstop layer after CMP, any post CMP cleans and

pre-etchstop deposition cleans are performed. Prior to striking a plasma in the chamber to begin SiN deposition, the semiconductor body is heated to approximately 425°C and SiH_4 (silane) gas is allowed to flow into the chamber and contact the surface of copper interconnect 100. Allowing the silane gas to flow for a few (0.5 to 5) seconds prior to striking the plasma (i.e., with the RF power still off), dopes the surface of the copper interconnect with silicon. For example, flowing the silane gas at a rate of 670 sccms for approximately three seconds prior to striking the plasma results ultimately in a silicon doping of approximately 0.1% for trench depths of ~ 0.45 microns. Silicon doping in the range of 0.03 at. % to 0.5 at. % is desired. Various methods for doping the surface of copper interconnect 100 will be apparent to those of ordinary skill in the art having reference to this specification.

[0026] It should be noted that the doping levels of the instant invention do not result in silicidation at the copper surface. At ~400°C, the solid solubility limit of Si in pure Cu is ~ 8 at. %. This is well above the levels of the instant invention. The duration of the exposure to SiH_4 is short (on the order of 3 sec.) in the instant invention, whereas normal silicidation exposure times are much longer (e.g., greater than 5 min.).

[0027] It should also be noted that Si doping negatively impacts resistivity of the copper interconnect. The resistivity increase depends on the final doping concentration which, in turn, depends on film thickness.

[0028] After doping the surface of the copper interconnect 100 to the desired level, a plasma is struck in the chamber and a SiN etchstop layer 120 is deposited as shown in FIG. 3E. As illustrated in Fig. 6 and discussed above, silicon doping of the copper interconnect improves SiN adhesion to the copper surface. Processing may then continue to form the next metal interconnect level (i.e., a second ILD, IMD, trench, vias, barrier, and copper), any additional metal interconnect levels and to package the device.

[0029] While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.